What is Claimed is:

1. A programmable logic device integrated circuit clock and data recovery circuit that recovers digital data and an embedded clock from an incoming serial data stream, the clock and data recovery circuit comprising:

a first phase-locked loop that locks onto a reference clock when the clock and data recovery circuit is operated in a reference mode;

a second phase-locked loop that locks onto the incoming serial data stream when the clock and data recovery circuit is operated in a data mode; and

a control circuit that automatically switches the clock and data recovery circuit between the reference mode and the data mode.

2. The programmable logic device integrated circuit clock and data recovery circuit defined in claim 1 wherein the control circuitry is responsive to an override signal that forces the clock and data recovery circuit out of the automatic mode and into the reference mode.

3. The programmable logic device integrated circuit clock and data recovery circuit defined in claim 1 wherein the control circuitry is responsive to an override signal that forces the clock and data recovery circuit out of the automatic mode and into the data mode.

4. The programmable logic device integrated circuit clock and data recovery circuit defined in claim 1 further comprising:

a charge pump having switch circuitry, wherein the control circuit switches the switch circuitry to use the charge pump in the first phase-locked loop or the second phase-locked loop depending on whether the clock and data recovery circuit is in the reference mode or the data mode.

5. The programmable logic device integrated circuit clock and data recovery circuit defined in claim 1 further comprising switch circuitry, wherein the control circuit includes circuitry responsive to a lock-to-data override signal and wherein when the lock-to-data override signal is asserted, the control circuitry directs the switch circuitry to switch the second phase-locked loop into use.

6. The programmable logic device integrated circuit clock and data recovery circuit defined in claim 1 further comprising switch circuitry, wherein the control circuit includes circuitry responsive to a lock-to-reference override signal and wherein when the lock-to-reference override signals is asserted, the control circuitry directs the switch circuitry to switch the first phase-locked loop into use.

7. The programmable logic device integrated circuit clock and data recovery circuit defined in claim 1 wherein the control circuit is controlled by a static override signal from a programmable element that has been configured using configuration data and wherein the static override signal is asserted to place the clock and data recovery circuit in the reference mode or is asserted to place the clock and data recovery circuit in the data mode.

8. The programmable logic device integrated circuit clock and data recovery circuit defined in claim 1 wherein the control circuit is controlled by a dynamic override signal from programmable logic device core logic on a programmable logic device and wherein the dynamic override signal is asserted to place the clock and data recovery circuit in the reference mode or is asserted to place the clock and data recovery circuit in the data mode.

9. The programmable logic device integrated circuit clock and data recovery circuit defined in claim 1 wherein the control circuit is responsive to an external override signal from a programmable logic device input pin and wherein the external override signal is asserted to place the clock and data recovery circuit in the reference mode or is asserted to place the clock and data recovery circuit in the data mode.

10. The clock and data recovery circuit defined in claim 1 wherein the first phase-locked loop includes:

a phase/frequency detector that has a reference clock input that receives the reference clock and a feedback clock input that receives a feedback clock, wherein the phase/frequency detector produces an output signal at its output that is indicative of whether the feedback clock matches the reference clock;

a charge pump that receives the output signal and produces a corresponding control signal;

a loop filter that filters the control signal from the charge pump and produces a corresponding loop filter output; and

a voltage-controlled oscillator that receives the loop filter output and produces a corresponding feedback signal at its output on which the feedback clock is based.

11. The clock and data recovery circuit defined in claim 10 wherein the second phase-locked loop includes a phase detector that has a data input at which the data stream is received, wherein the phase detector has a phase detector output coupled to the charge pump, wherein the charge pump has switch circuitry responsive to a control signal from the control circuit, wherein the switch circuitry switches either the phase/frequency detector output signal or the phase detector output into the charge pump, and wherein the control circuit

switches the first phase-locked loop or the second phase-locked loop into use by using the control signal to control the switch circuitry in response to override signals.

12. An integrated circuit clock and data recovery circuit that recovers digital data and an embedded clock from an incoming serial data stream, the clock and data recovery circuit comprising:

a first phase-locked loop that locks onto a reference clock when the clock and data recovery circuit is operated in a reference mode;

a second phase-locked loop that locks onto the incoming serial data stream when the clock and data recovery circuit is operated in a data mode; and

a control circuit that operates in an automatic mode in which the control circuit automatically switches the clock and data recovery circuit between the reference mode and the data mode, wherein when the control circuit receives an override signal, the control circuit exits the automatic mode.

13. The integrated circuit clock and data recovery circuit defined in claim 12 further comprising switch circuitry, wherein the first phase-locked loop produces a feedback signal and wherein when the override signal is received by the control circuit, the control circuit directs the switch circuitry to switch the first phase-locked loop into use so that the feedback signal

is locked to the reference clock by the first phase-locked loop.

14. The integrated circuit clock and data recovery circuit defined in claim 12 further comprising switch circuitry, wherein the second phase-locked loop produces a feedback signal and wherein when the override signal is received by the control circuit, the control circuit directs the switch circuitry to switch the second phase-locked loop into use so that the feedback signal is locked onto the incoming serial data stream by the second phase-locked loop.

15. The integrated circuit clock and data recovery circuit defined in claim 12 wherein the first and second phase-locked loops contain a shared charge pump having a switch circuit, a shared filter that filters charge pump output signals and produces corresponding filtered signals, and a shared oscillator that is controlled by the filtered signals, and wherein the first phase-locked loop comprises a phase/frequency detector that compares the reference clock to a feedback clock signal that is generated using the oscillator.

16. The integrated circuit clock and data recovery circuit defined in claim 12 wherein the first and second phase-locked loops contain a shared charge pump having a switch circuit, a shared filter that filters charge pump output signals and produces

corresponding filtered signals, and a shared oscillator that is controlled by the filtered signals, and wherein the second phase-locked loop comprises a phase detector circuit that compares the incoming serial data stream clock to a feedback clock signal that is generated using the oscillator.

17. The integrated circuit clock and data recovery circuit defined in claim 12 further comprising at least one detector that produces at least one signal indicative of whether the first phase-locked loop has locked onto the reference clock, wherein the control circuit uses that at least one signal in automatically moving the clock and data recovery circuit from reference mode to data mode.

18. The integrated circuit clock and data recovery circuit defined in claim 12 further comprising at least one detector that produces a detector output that is indicative of whether the first phase-locked loop has locked onto the reference clock, wherein the control circuit uses the detector output to decide when to automatically move the clock and data recovery circuit from reference mode to data mode when the clock and data recovery circuit is in the automatic mode and wherein, when the override signal is received, the control circuit disregards the detector output and exits the automatic mode to place the clock and data recovery circuit in reference mode using the first phase-locked

loop to lock onto the reference clock.

19. The integrated circuit clock and data recovery circuit defined in claim 12 further comprising at least one detector that produces a detector output that is indicative of whether the first phase-locked loop has locked onto the reference clock, wherein the control circuit uses the detector output to decide when to automatically move the clock and data recovery circuit from reference mode to data mode when the clock and data recovery circuit is in the automatic mode and wherein, when the override signal is received, the control circuit disregards the detector output and exits the automatic mode to place the clock and data recovery circuit in data mode using the second phase-locked loop to lock onto the incoming serial data stream.

20. A programmable logic device, comprising:

a programmable element whose static programmed state is determined by loading configuration data into the programmable element from a source external to the programmable logic device, wherein when the programmable element is in its static programmed state, the programmable element produces a static control signal;

a clock and data recovery circuit that recovers digital data and an embedded clock from an incoming serial data stream that is provided to the programmable logic device from a communications link,

the clock and data recovery circuit including:

a first phase-locked loop that locks onto a reference clock when the clock and data recovery circuit is operated in a reference mode;

a second phase-locked loop that locks onto the incoming serial data stream when the clock and data recovery circuit is operated in a data mode;

at least one detector that produces a detector output that is indicative of whether the first phase-locked loop has locked onto the reference clock; and

a control circuit that, when the clock and data recovery circuit operates in an automatic mode, automatically switches the clock and data recovery circuit between the reference mode and the data mode based at least partly on the detector output, wherein the static control signal from the programmable element is used as an override signal that directs the control circuit to exit the automatic mode and to place the clock and data recovery circuit in a given one of either the reference mode or the data mode, regardless of the detector output.

21. The programmable logic device of claim 20 further comprising core logic that has been programmed to implement a process, wherein the process produces at least one dynamic override signal that is provided to the control circuit to cause the control circuit to exit

the automatic mode.

22. The programmable logic device of claim 20, wherein the clock and data recovery circuit includes switch circuitry that the control circuit uses to switch either the first or second phase-locked loop into use depending on whether the clock and data recovery circuit is in the reference mode or the data mode, wherein the control circuit comprises logic that receives a lock-to-reference override signal and a lock-to-data signal and that produces a corresponding output control signal, wherein when the lock-to-reference signal is asserted, the control circuit adjusts the output control signal to direct the switch circuitry to switch the first phase-locked loop into use and when the lock-to-data signal is asserted, the control circuit adjusts the output control signal to direct the switch circuitry to switch the second phase-locked loop into use.

23. A method for controlling a programmable logic device integrated circuit clock and data recovery circuit comprising:

implementing a process in programmable core logic on a programmable logic device by loading configuration data into the programmable logic device, wherein the process produces a dynamic override signal; and

using the clock and data recovery circuit to either lock onto a reference clock or to lock onto an

incoming serial data stream, wherein using the clock and data recovery circuit comprises:

in an automatic mode, automatically switching the clock and data recovery circuit back and forth repeatedly between a first mode in which the clock and data recovery circuit locks onto the reference clock and a second mode in which the clock and data recovery circuit locks onto the incoming serial data stream; and

in response to the dynamic override signal, exiting the automatic mode and placing the clock and data recovery circuit into either the first mode or the second mode.

24. The method defined in claim 23 wherein using the clock and data recovery circuit to either lock onto the reference clock or to lock onto the incoming serial data stream comprises using a first phase-locked loop in the clock and data recovery circuit to lock onto the reference clock or using a second phase-locked loop in the clock and data recovery circuit to lock onto the incoming serial data stream.

25. The method defined in claim 23 wherein the process comprises an oversampling process that generates a lock-to-reference override signal and wherein exiting the automatic mode comprises exiting the automatic mode to place the clock and data recovery circuit into the first mode in response to the lock-to-reference override signal.

26. The method defined in claim 23 wherein the process produces a lock-to-date override signal and wherein exiting the automatic mode comprises exiting the automatic mode to place the clock and data recovery circuit into the second mode in response to the lock-to-date override signal.